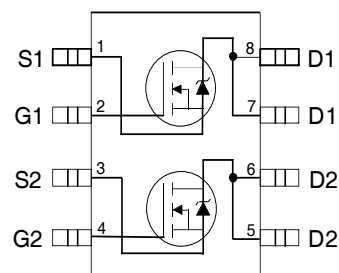


Features

- $V_{DS} = 50V$
- $R_{DS(ON)} < 30m\ \Omega$ ($V_{GS} = 10V$)
- $R_{DS(ON)} < 40m\ \Omega$ ($V_{GS} = 4.5V$)
- Advanced Process Technology
- Ultra Low On-Resistance
- Surface Mount
- Dynamic dv/dt Rating
- Fast Switching
- Lead-Free



Top View

Description

The SOP-8 has been modified through a customized leadframe for enhanced thermal characteristics and dual-die capability making it ideal in a variety of power applications. With these improvements, multiple devices can be used in an application with dramatically reduced board space. The package is designed for vapor phase, infra red. or wave soldering techniques. Power dissipation of greater than 0.8W is possible in a typical pcB mount application.

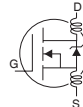
Absolute Maximum Ratings

	Parameter	Max.	Units
$I_D @ T_A = 25^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	3.0	A
$I_D @ T_A = 70^\circ C$	Continuous Drain Current, $V_{GS} @ 10V$	2.3	
I_{DM}	Pulsed Drain Current ①	10	
$P_D @ T_A = 25^\circ C$	Power Dissipation	2.0	W
	Linear Derating Factor	0.016	W/°C
V_{GS}	Gate-to-Source Voltage	± 20	V
dv/dt	Peak Diode Recovery dv/dt ②	4.5	V/nS
T_J, T_{STG}	Junction and Storage Temperature Range	-55 to + 150	°C

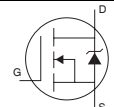
Thermal Resistance Ratings

	Parameter	Min.	Typ.	Max.	Units
$R_{\theta JA}$	Maximum Junction-to-Ambient ④			62.5	°C/W

Electrical Characteristics @ $T_J = 25^\circ\text{C}$ (unless otherwise specified)

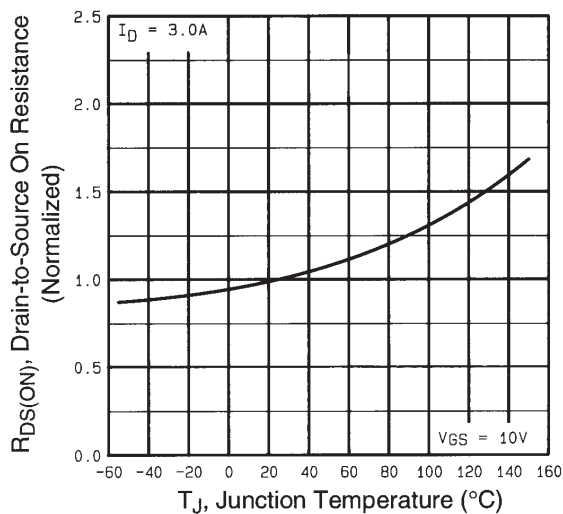
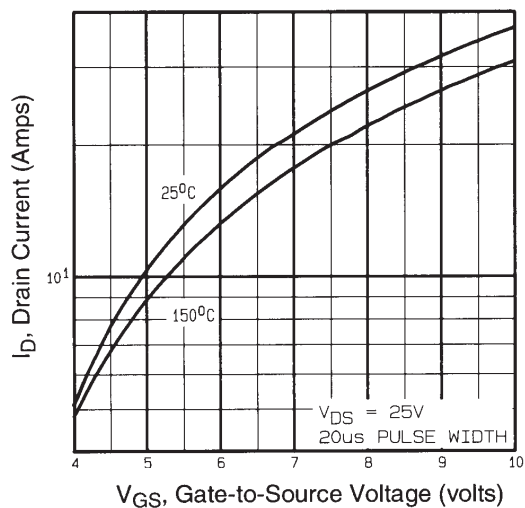
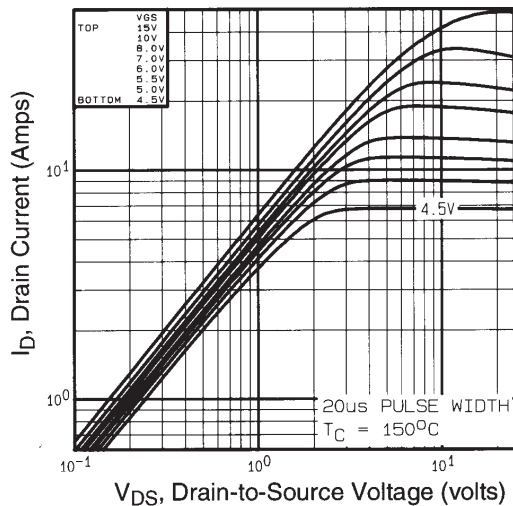
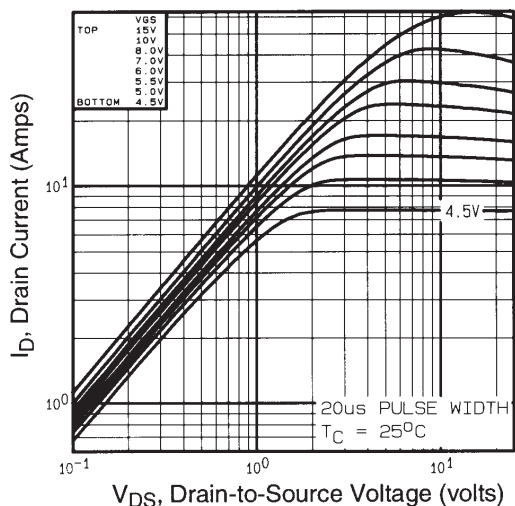
	Parameter	Min.	Typ.	Max.	Units	Conditions
$V_{(BR)DSS}$	Drain-to-Source Breakdown Voltage	50			V	$V_{GS} = 0V, I_D = 250\mu A$
$\Delta V_{(BR)DSS}/\Delta T_J$	Breakdown Voltage Temp. Coefficient		0.049		V/ $^\circ\text{C}$	Reference to 25°C , $I_D = 1mA$
$R_{DS(ON)}$	Static Drain-to-Source On-Resistance		21 32	30 40	$m\Omega$	$V_{GS} = 10V, I_D = 3.0A$ ③ $V_{GS} = 4.5V, I_D = 1.5A$ ③
$V_{GS(th)}$	Gate Threshold Voltage	1.0		3.0	V	$V_{DS} = V_{GS}, I_D = 250\mu A$
g_{fs}	Forward Transconductance		3.8		S	$V_{DS} = 15V, I_D = 3.0A$ ③
I_{DSS}	Drain-to-Source Leakage Current			2.0 25	μA	$V_{DS} = 40V, V_{GS} = 0V$ $V_{DS} = 40V, V_{GS} = 0V, T_J = 55^\circ\text{C}$
I_{GSS}	Gate-to-Source Forward Leakage			100	nA	$V_{GS} = 20V$
	Gate-to-Source Reverse Leakage			-100	nA	$V_{GS} = -20V$
Q_g	Total Gate Charge		12	30	nC	$I_D = 2.0A$
Q_{gs}	Gate-to-Source Charge		1.2		nC	$V_{DS} = 25V$
Q_{gd}	Gate-to-Drain ("Miller") Charge		3.5		nC	$V_{GS} = 10V$ ③
$t_{d(on)}$	Turn-On Delay Time		9.0	20	ns	$V_{DD} = 25V$ $I_D = 1.0A$ $R_G = 6.0\Omega$ $R_D = 25\Omega$ ③
t_r	Rise Time		8.0	20		
$t_{d(off)}$	Turn-Off Delay Time		45	70		
t_f	Fall Time		25	50		
L_D	Internal Drain Inductance		4.0		nH	Between lead, 6mm (0.25in.) from package and center of die contact 
L_S	Internal Source Inductance		6.0			
C_{iss}	Input Capacitance		290		pF	$V_{GS} = 0V$ $V_{DS} = 25V$ $f = 1.0MHz$
C_{oss}	Output Capacitance		140			
C_{rss}	Reverse Transfer Capacitance		37			

Source-Drain Ratings and Characteristics

	Parameter	Min.	Typ.	Max.	Units	Conditions
I_S	Continuous Source Current (Body Diode)			2.0	A	MOSFET symbol showing the integral reverse p-n junction diode. 
I_{SM}	Pulsed Source Current (Body Diode) ①			12		
V_{SD}	Diode Forward Voltage			1.2	V	$T_J = 25^\circ\text{C}, I_S = 1.5A, V_{GS} = 0V$ ③
t_{rr}	Reverse Recovery Time		70	100	ns	$T_J = 25^\circ\text{C}, I_F = 1.5A$
Q_{rr}	Reverse Recovery Charge		110	170	nC	$di/dt = 100A/\mu s$ ③
t_{on}	Forward Turn-On Time		Intrinsic turn-on time is negligible (turn-on is dominated by $L_S + L_D$)			

Notes:

- ① Repetitive rating; pulse width limited by max. junction temperature.
- ② $I_{SD} \leq 1.8A$, $di/dt \leq 90A/\mu s$, $V_{DD} \leq V_{(BR)DSS}$, $T_J \leq 150^\circ\text{C}$
- ③ Pulse width $\leq 300\mu s$; duty cycle $\leq 2\%$.
- ④ Surface mounted on FR-4 board, $t \leq 10sec$.



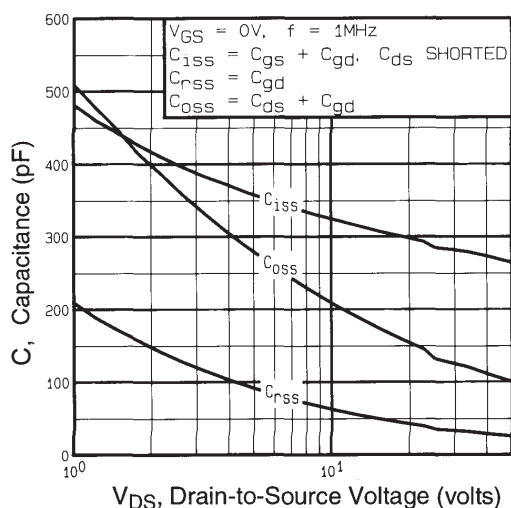


Fig 5. Typical Capacitance Vs. Drain-to-Source Voltage

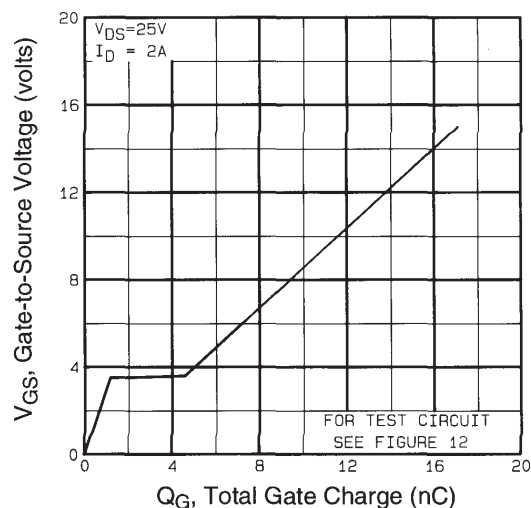


Fig 6. Typical Gate Charge Vs. Gate-to-Source Voltage

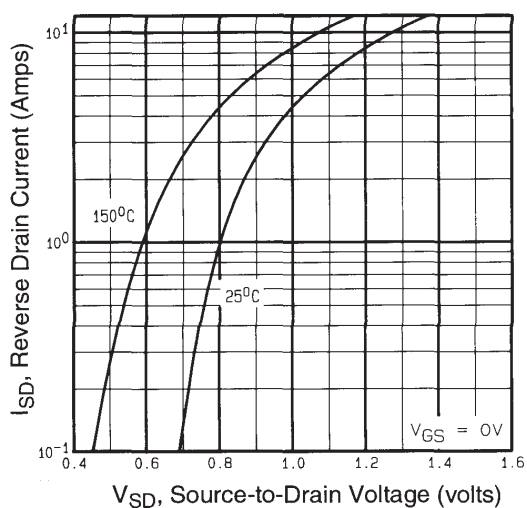


Fig 7. Typical Source-Drain Diode Forward Voltage

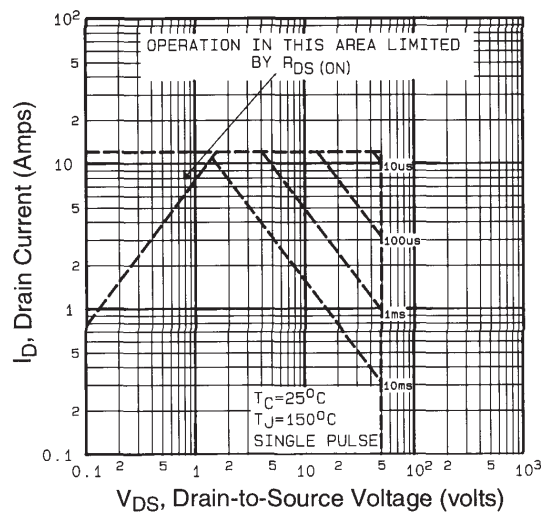


Fig 8. Maximum Safe Operating Area

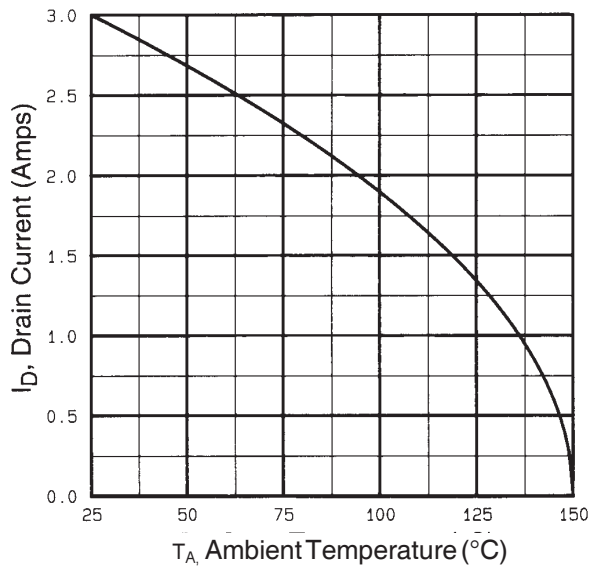


Fig 9. Maximum Drain Current Vs. Ambient Temperature

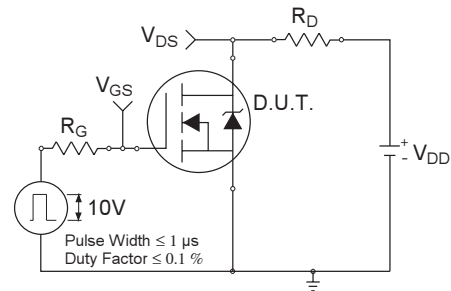


Fig 10a. Switching Time Test Circuit

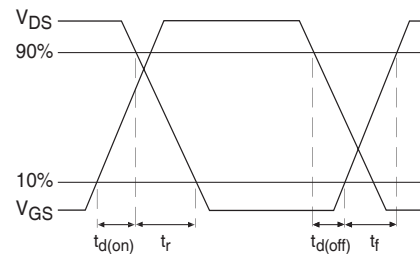


Fig 10b. Switching Time Waveforms

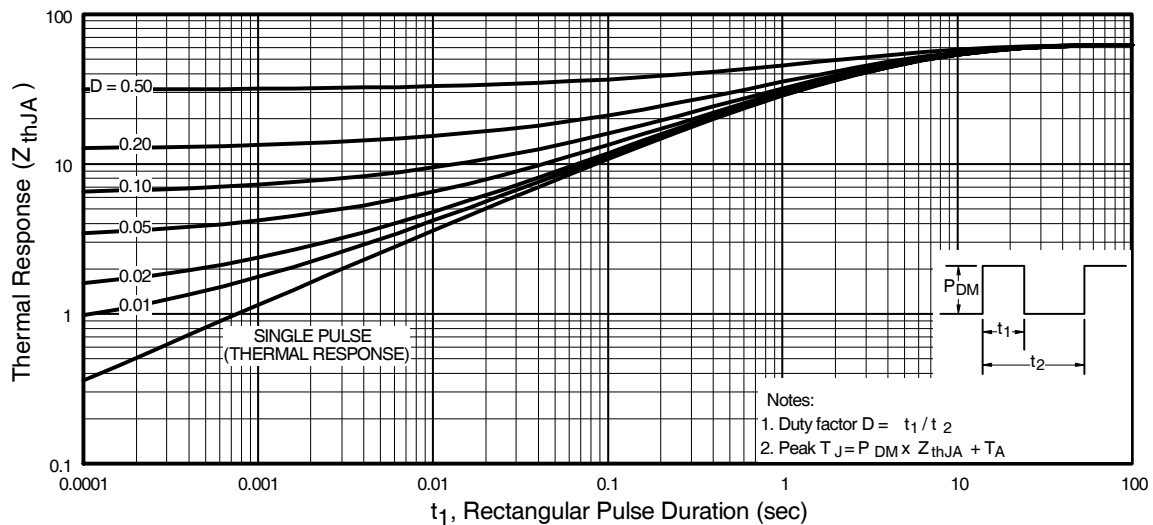


Fig 11. Maximum Effective Transient Thermal Impedance, Junction-to-Ambient

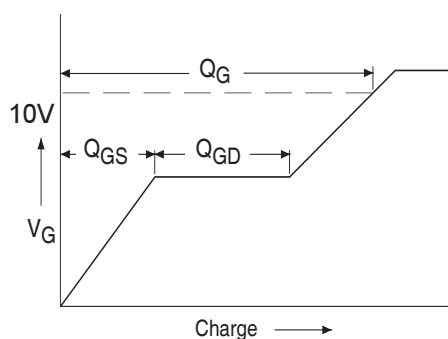


Fig 12a. Basic Gate Charge Waveform

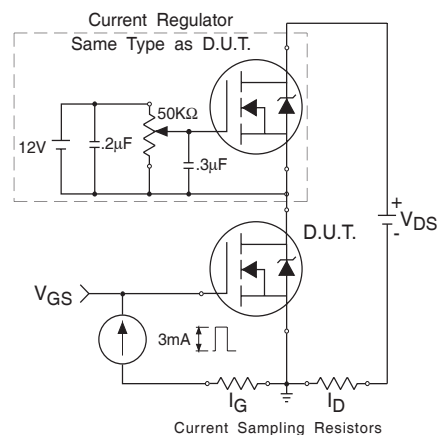
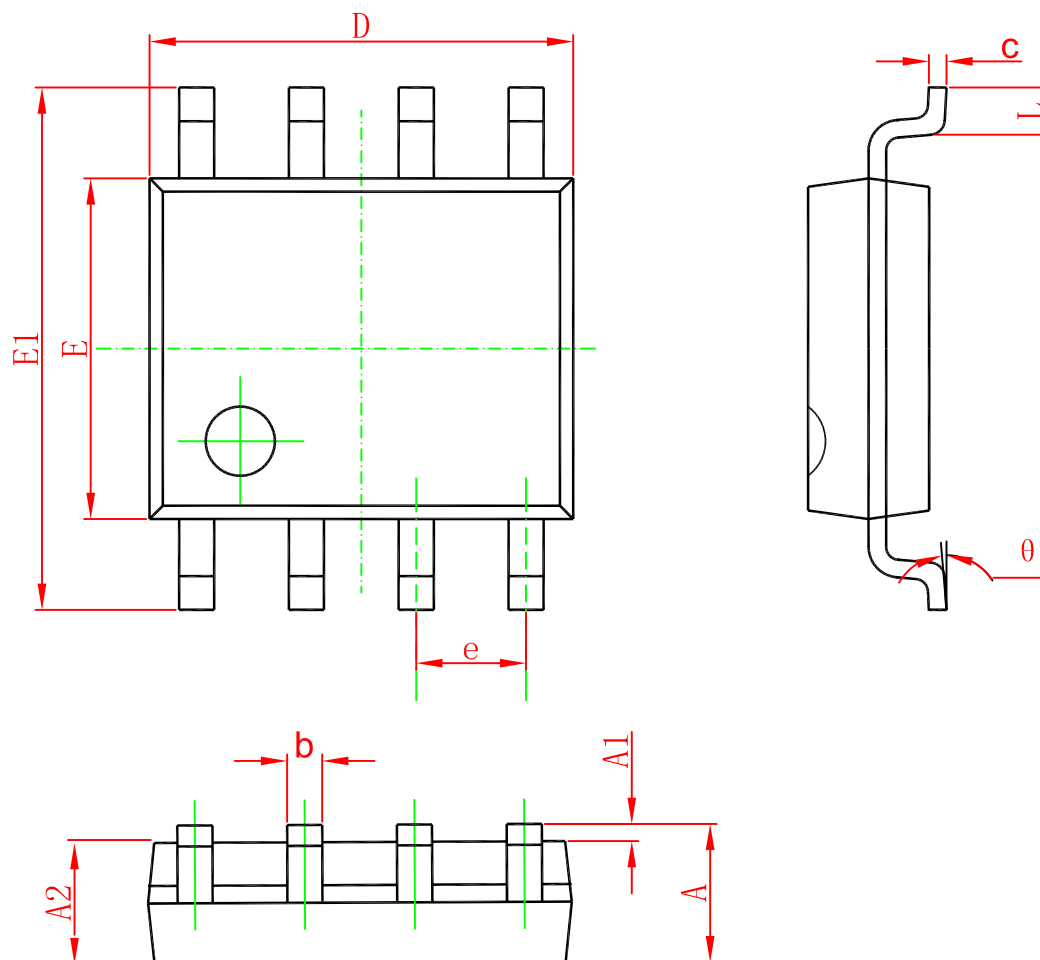
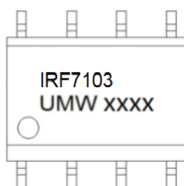


Fig 12b. Gate Charge Test Circuit



Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min	Max	Min	Max
A	1.350	1.750	0.053	0.069
A1	0.100	0.250	0.004	0.010
A2	1.350	1.550	0.053	0.061
b	0.330	0.510	0.013	0.020
c	0.170	0.250	0.006	0.010
D	4.700	5.100	0.185	0.200
E	3.800	4.000	0.150	0.157
E1	5.800	6.200	0.228	0.244
e	1.270(BSC)		0.050(BSC)	
L	0.400	1.270	0.016	0.050
θ	0°	8°	0°	8°

Marking



Ordering information

Order code	Package	Baseqty	Deliverymode
UMW IRF7103TR	SOP-8	3000	Tape and reel